Advanced Computer Structure Lab

Lab organization:

The Advanced Computer Structure Lab is held weekly and is built of Recitations and Lab meetings.

Every Recitation lasts 2 hours and is held before the corresponding Lab meeting, for all the students at once in usual class room. For some of the Lab handouts to be completed takes one Recitation, but more than one Lab meeting.

The Lab meetings are of 3 hours each and are held in Lab room 204, Classes building. Students are working in pairs and at most 5 pairs occupy the Lab at once.

The Lab is completed after reporting the multiple assignments and passing the two short (up to 90 minutes) quizzes. Each assignment is composed of pre-lab and post-lab reports. First quiz (Midtherm) is held after the first 5 assignmets are compleated, the second(Final) – in the last two weeks of the exam's period.

The exact schedule of Recitations, Lab meetings and Quizzes is presented in the Labs site.

In case the Lab will be held in remote mode, SKYPE and ANYDESK are used to support the Lab communication and quizzes can be replaced by remote personal examination.

Course Topics:

- Introduction (2 recitations and 2 Lab meetings).

  Lab organization and administration, user accounts and computer set up.

  Installation, configuration and licensing of the Xilinx design software (ISE v14.7) at home computer. Usage of the Xilinx ISE software installed in computer classes.

  Short description of Digital Design implementation, FPGA structure and configuration.

  Introduction to Computer aided hardware design and simulation. How to use the Xilinx ISE to prepare hardware designs and how to test the correctness of designs (i.e. simulation).

  Logical structure of the educational RESA Computer (board with Xilinx FPGA) with their buses and protocols. Read and Write transactions over the bus. Design and simulation of the CPU bus interface.

- Monitoring tools (2 recitations and 3 Lab meetings).

  Introduction to the RESA board architecture. How to create a configuration file for the FPGA (i.e. implementation). How to: run the RESA monitoring program and using it to configure FPGA, upload program codes and debug the design.

  Design and simulation of Simple slave device. Implementation and hardware debugging of the design using RESA Computer (target FPGA board and monitoring program).

  Design and simulation of Hardware Monitor, consisting of Simple slave, ID and Build-in Logic analyzer. Design implementation and hardware debugging using RESA Computer. Analyzing the monitoring results for few steps.

  First quiz (Midtherm) with questions based on the passed Handouts.

- Main part (6 recitations and 8 Lab meetings).

  Read and Write transactions to the External Memory. Design, simulation and implementation of Read and Write machines. Debug the designs using previously designed Hardware Monitor with the Logic analyzer.

  Design of Load/Store machine with Control and Data Path. Simulation of the Control using test vectors. I/O Simul structure and initialization data. How to use the Assembly Editor/Compiler and the CPU Simulator. How to use the I/O Simul to simulate and debug the RTL and whole instructions. Implementation and debug of the Load/Store Machine with the RESA Computer.

  Design and simulation of Simplified DLX RISC CPU. Writing short test programs in Assembly and updating the initialization data of I/O Simul. Implementation and debug of the CPU using student's test programs. Final QA with CPU's Lab test program. Timing issues and work around the timing

optimization.

Write an assembly program, that solves a given problem, and run it on your previously designed DLX CPU.

Second quiz (Final) with questions based on the Load/Store machine and DLX CPU Handouts.